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Recycling rejected silicon wafers and dies for high grade PV cells

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Exponential growth in solar panel production and energy storage solutions has resulted in pressure on the supply of solar cell materials. Another environmental challenge stems from the fact that panels installed in the 90s and the beginning of the 2000s have reached their end of life and are being discarded in landfills. Hence, in this work, we focus on recycling silicon wafers and dies by stripping previous structures from the die using potent acids, after which its base material is characterized and binned. We demonstrate the process for silicon p-type substrates where n-type doping is attained by using a simple solution of phosphoric acid, which is diffused into the substrate using a furnace, thus creating a PN junction. If the substrate is n-type, it could be replaced by boric acid. This is followed by deposition of a conductive antireflective coating, bus bars, and rear wafer metal coating. The initial demonstrated laboratory results indicate the feasibility of recycling wafers using simple, low-cost standard industrial methods.

Keywords: PV, Silicon Recycling, solar cell recycling

INTRODUCTION

Renewable energy sources for electrical energy generation have become an increasing concern in most countries due to the environmental impact associated with the use of fossil fuels. In addition, reducing a country's dependence on fossil fuel further increases its self-reliance and improves a nations balance of trade, thus boosting its economy. Some countries have initiated programs increasing economic incentives to companies and individual households for developing, improving efficiencies, or increasing the capacity of renewal energy sources. In a recent report [1] the International Renewable Energy Agency estimates the current cost of PV electrical generation at optimal locations, has reached prices that are comparable to the lower end of fossil fuel costs. The various steps of manufacturing solar panels from raw materials are energy-intensive and include the use of large amounts of water and toxic chemicals. Therefore, expecting the rapid growth of silicon used for solar energy generation since the late 90s of the previous century, research was conducted for initiating environmentally benign solar cell manufacturing [2]. The predicted increase in solar panel production and installations [1] and the 25-year life expectancy of a solar panel have initiated various End of Life (EOL) management programs [3-6].

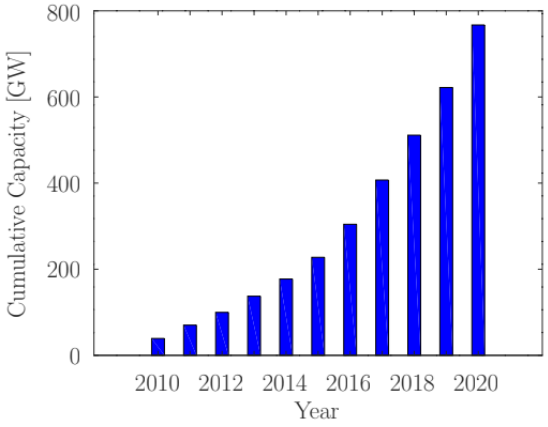

Fig.1. Cumulative capacity exponential growth between 2010 and 2020, based on [7]

The exponential growth of solar energy generation (Fig.1.) having a capacity of 39.2 GW in 2010, rapidly increasing to 767.2 GW in 2020, and expected to rise to 4,500GW by 2050 [6] will lead to an increase in PV panel waste. The move to a carbon-free and more sustainable energy production is being championed by PV-based solar panels. As production has been increasing exponentially in the past two decades, recycling the raw materials from the fabs and end-of-life panels is of prime importance. Understanding the negative impact of the PV waste and trying to limit it, the EU has decided to include PV panels in the waste of electrical and electronic equipment directive (WEEE). The US is expected to follow soon (Some states have adopted the European WEEE). As a result PV manufacturers and distributors are legally required to collect and recycle end-of-life PV

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products. Most silicon solar cells are based on single-crystal silicon (monocrystals) grown by the Czochralski technique and polycrystalline silicon casting. While there are more efficient materials for photovoltaic energy generation than single-crystal silicon, they are not commercially viable for large area applications. In 2015, crystalline silicon had approximately 93% of the market share of solar modules, with 24% going to the monocrystals and 69% going to the polycrystalline solar cells [8]. The larger market share of the polycrystalline solar cells is due to the significantly lower production costs, but this comes at a price of lower efficiency compared to the single crystal silicon. For most uses, where space or weight is not a concern the polycrystalline solar cells are appropriate. In places where space and weight are restricted, single crystal silicon, due to its higher efficiency is better suited. When dealing with monocrystal-based photovoltaic cells, higher-quality crystals result in higher conversion efficiency, but it comes at an economical price. Integrated circuit grade silicon is probably the most efficient base material for fabricating silicon solar panels due to its low defect density, but the lengths and costs for obtaining it are prohibitive for its wide application in terrestrial energy generation, where the capital investment per Watt is the key driving force. To reduce costs solar grade silicon monocrystals with a much higher level of defects and impurities are being introduced [9]. Another concern that needs to be addressed is the recycling of the panels when they reach their end of life (EOL). In this respect, rare metals and silicon cells retain their value and should be salvaged using various techniques [4,5]. One untapped resource of high quality near defect-free silicon is rejected dies and wafers. With an estimated 90% yield during full production [10] we are left with 10% rejected dies. Currently, state-of-the-art fabs are producing integrated circuits with wafer diameters of 300 mm (12") while the next standard size for such fabs, is projected to be 450 mm (18"). This provides an abundant supply of silicon for producing high-quality solar panels. In this article, we will present a relatively environmentally friendly method for recycling silicon from the rejected wafers.

MATERIALS PREPARATION

This work based on experiments conducted by our groups, suggests a method for recovering rejected silicon dies, wafers and residual silicon which resides on the rims of the processed wafers. In order to keep the text clear, we shall generally refer to all the recovered silicon as dies. The process results in PN photovoltaic structures composed of In_2O_5Sn / *n-Si* / *p-Si* (ITO,n-type silicon, p-type silicon).

Stripping

The dies were etched in after which the conductivity and type were measured. This assists us with defining the type of base material to deposit prior to diffusion (Phosphorous/Arsenic or Boron/Gallium). Similar die types are binned together. In this article we shall describe the process for a p-type substrate. Standard cleaning recipe was applied to the dies with an optional oxide strip using between the first step (SC-1) and the second step (SC-2). When using those steps, the rare metals can be recovered using the processes described in [4].

Donor/Acceptor diffusion

The samples were spin coated using a solution of 1:1 ratio of phosphoric acid and ethanol (H_3PO_4:C_2H_5OH). If the substrate is n-type one can replace the phosphoric acid with boric acid (H_3BO_3). The samples were place in a furnace with an ambient atmosphere pre-baking them at a temperature of 150^{o}C for 10 minutes drying the newly applied coating. The temperature was raised to a temperature of 900^{o}C for 6 hours slowly cooling it to a level of 600^{o}C, this procedure allows for propper diffusion while reducing destructive glass phases. Dopant concentration was evaluated using ICP-OES [11] which can trace down to approximately $N_d \sim 10^{14}$ [cm^{-3}].

Transparent Conductive Oxide coating

Although much work was conducted in the past 20 years, on the topic of environmentally sustainable, indium free Transparent Conducting Oxides (TCOs), for example [12,13] , in this work we used ITO with the standard application methods. Transparent conductive films of In_2O_5Sn were deposited by RF sputtering using an ITO ceramic (90 wt% In_2O_3, 10 wt% SnO_2). Substrates were cleaned using ultra pure deionized water isopropyl alcohol and acetone in an ultrasonic cleaner bath for 20 minutes. This was followed by drying using a flow of nitrogen gas. The RF sputtering chamber was purged with Ar and a working pressure of 100 mTorr was maintained. Surface oxidation was removed in the pre-

sputtering stage. A film of approximately 250nm was deposited on the surface of the materials with the procedure tested using microscope slides prior to the actual deposition. The deposited film was annealed in a tube furnace in an oxygen saturated environment supported by a 0.5 sccm gas flow at a temperature of 400ºC. Optical transparency of the In_2O_5Sn films was measured in the UV/VIS using a Jasco V-730. Additionally, it was used in reflective mode to measure the film thickness [14] using the SLM-907 specular reflectance accessory. Fig.2. illustrates the transmission of the glass substrate and the ITO deposition on the glass substrate.

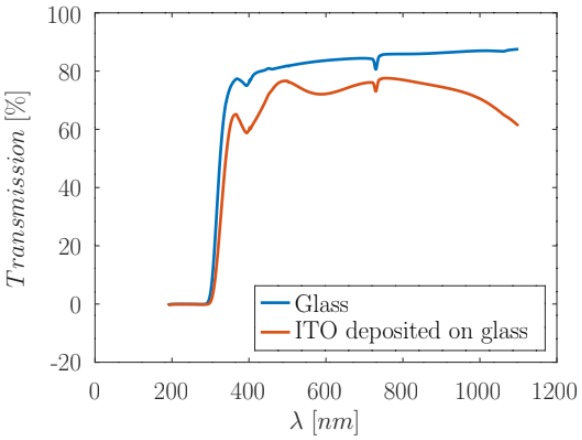

Fig.2. Optical transmission of the ITO on a glass substrate compared to the transmission of the glass substrate

The optical transmission of the ITO excluding the glass substrate in the 420-1100nm range is given in Fig.3.

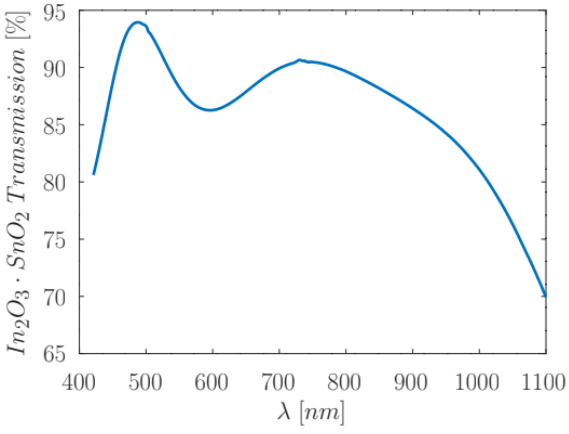

Fig.3. Optical transmission of the ITO excluding the glass substrate

As can be seen in Fig.3, the optical transmission at 500nm is 93.6% which compares favorably with published data [15,16]. Inkjet printing of the collector bus bar and finger aluminum electrodes were tested with inconclusive results. As a result we opted for the traditional method of applying aluminum electrodes by thermal evaporation deposition.

A four-point measurement of the In_2O_5Sn deposited layer resistance was conducted before and after the diffusion validating the resistivity of the layer. Fig.4. illustrates the resistivity obtained using three different samples from three different batches.

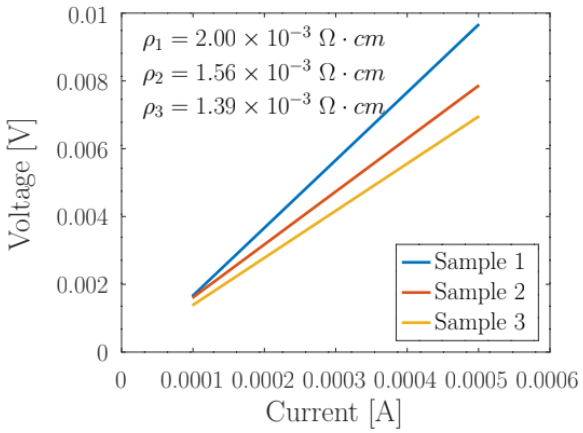

Fig.4. Resistivity of the ITO deposited layer of three different batches as extracted from a four point measurement

The resistivity results correspond with published data [16]. A hot probe experiment identified the type of semiconductor layer after the diffusion process a detailed account of the measurement can be found in [17]. During the various processes the surface structure was studied and documented using a metallurgical microscope.

EXPERIMENTAL RESULTS

A standard photovoltaic structure with a thin emitter fabricated at the top surface using a p-type substrate is demonstrated in Fig.5.

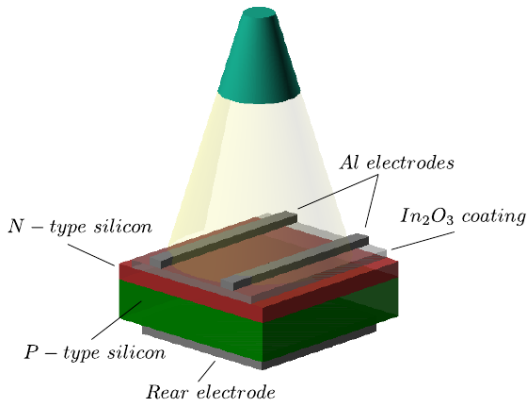

Fig.5. Photovoltaic cell structure

The wavelength dependent short circuit current is approximated by

$$J_{sc}(\lambda) = \frac{q\ (\lambda)(1-R_f)\alpha L_p}{\alpha^2 L_p^2 - 1}\Phi_e \qquad (1)$$

With Φ_e presenting an emitter factor which depends on doping levels and depth of doping:

$$\Phi_e = \frac{\frac{S_p L_p}{D_p} + \alpha L_p - e^{-\alpha H_e}\left(\frac{S_p L_p}{D_p}\cdot\cosh(h_e/L_p) + \sinh(h_e/L_p)\right)}{\frac{S_p L_p}{D_p}\sinh(h_e/L_p) + \cosh(h_e/L_p) - \alpha L_p e^{-\alpha H_e}\}} \qquad (2)$$

Where:

$\phi(\lambda)$	photon flux $[\#photons/sec\cdot m^2]$
R_f	reflectance of the active surface of the cell
α	absorption coefficient of the semiconducting material $[cm^{-1}]$
L_p	diffusion length of the minor charge carriers in the emitter $L_p = \sqrt{D_p \cdot \tau_p}$ $[cm]$
S_p	surface recombination velocity for minor charge carriers $[cm/s]$
h_e	depth of the emitter $[cm]$
D_p	diffusion coefficient of minor charge carriers in the emitter $[cm^2/s]$

$J_{ph} = q\cdot(\lambda)$ the photon flux current is referred to as the photon flux which is the current given that every photon generates an electron hole pair. In order to get a grasp of the behavior of the short circuit current Eq. (1) one has to observe that the emitter factor Eq. (2) has the form

$$\Phi_e \approx C - Be^{-t} \underset{t\to\infty}{\rightarrow} C \qquad (3)$$

In which C is a constant depending on the minor charge carrier attributes (L_p, D_p) which are donor density dependent, the depth h_e and the surface recombination velocity S_p. The surface recombination velocity depends on both the surface defects and doping levels. For a passivated surface the doping level is Ns ≈ $10^{18} - 10^{19}$. The surface recombination velocity is given by [18, 19]

$$S_p = 10^{-16} N_s \qquad (4)$$

Fig.6 shows the calculated short circuit current as a function of the depth of the emitter.

For the above parameters it can be seen that the optimal depth of the emitter is approximately 3μm. The current is wavelength dependent on three accounts. Two external ones which are the photon flux, and the reflection R_f and an internal one being the absorption coefficient α.

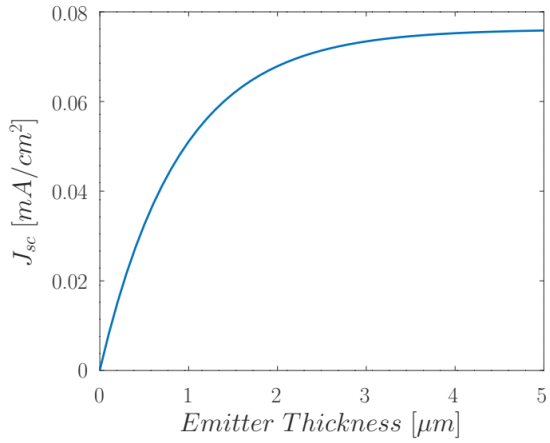

Fig.6. Short circuit current as a function of the depth of the emitter for: λ = 500nm; R_f (λ) = 0.05 α(λ) = 1.11 ×10^4 ; S_p = 200 [cm/s]; D_p = 13 [cm^2 /s]; τ_p = 10μs; J_{ph}(λ) = 0.08 [mA/cm^2]

Reflectance

R_f is a significant parameter as it has a considerable influence on the efficiency of the PV cell as is seen in Eq. (1). On bare silicon R_f > 30% reducing the efficiency considerably. In order to decrease the reflection loss in the visible and NIR range an anti-reflective coating is applied. The applied coating needs to shift the phase of the reflected light by half a wavelength, thus canceling each other out. This happens when the surface of the silicon and the applied coating are at a distance of λ/4, or

$$n_c d = \lambda/4 \qquad (5)$$

A further improvement (minimization of reflection losses) is obtained when the coating is the mean of the refractive indices i.e.

$$n_c(\lambda) = \sqrt{n_{air}\cdot n_{Si}} \qquad (6)$$

$$n_c(500nm) \approx 2.11$$

One such material that is both transparent and which provides an appropriate solution over most of the visible range is ITO. Fig.7 displays the refractive index and the square root of the refractive index of the silicon compared to the refractive index of ITO.

Our peak wavelength is about 500nm and according to the graph n_{ITO} (500) ≈ 2 thus a deposition thickness of 125nm is appropriate for our purpose. As was seen in Fig.3, the low

resistivity of the ITO film on our samples accommodates the conduction of charge to the fingers and bus bars.

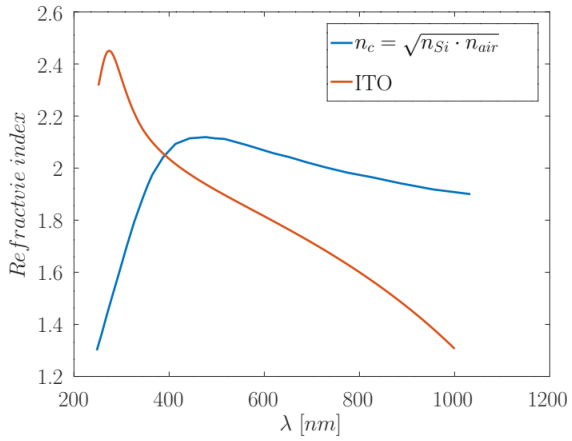

Fig.7. Comparison between the index of refraction of ITO and the square root of n_{Si} and n_{air}

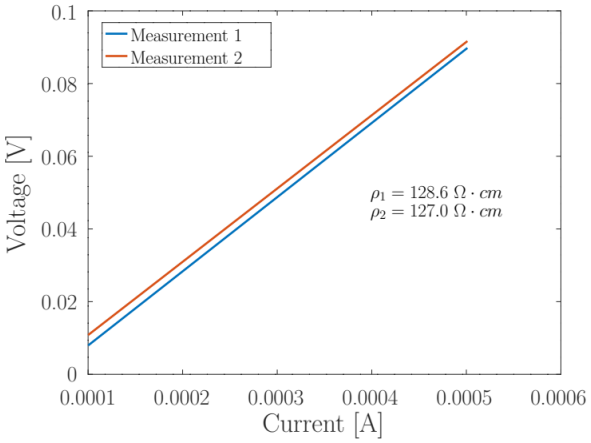

Fig.8. A four point measurement of the doped (emitter) layer

Post diffusion

The describe process's weakness is that, to date, it is not a completely controlled process. While during the classic method the flow of the dopant gas is controlled, some of the spin coated material evaporates and we need to resort to ICP-OES measurements in order to estimate dopant concentration. The resistivity of the doped layer was measured using a four point measurement as shown in Fig.8.

The resistivity result of ~127Ω · cm corresponds with a dopant density of 4×10^{14} cm^{-3} [20] which was confirmed by the ICP-OES measurement which is approximately 5×10^{14} cm^{-3} (close to the detection limit of the phosphorus). Following the resistivity characterization the I-V characteristic was measured at different temperatures. Fig.9 indicates that the material displays a regular PN junction behaviour.

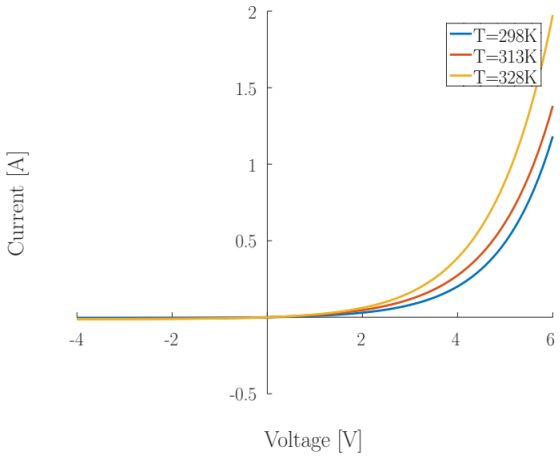

Fig.9. Device I-V characteristic at several temperatures

The calculated potential of the junction is 0.5 V while the actual open circuit voltage was found to be lower than 0.1 V. This is due to the high losses in this device which is in its preliminary research stages.

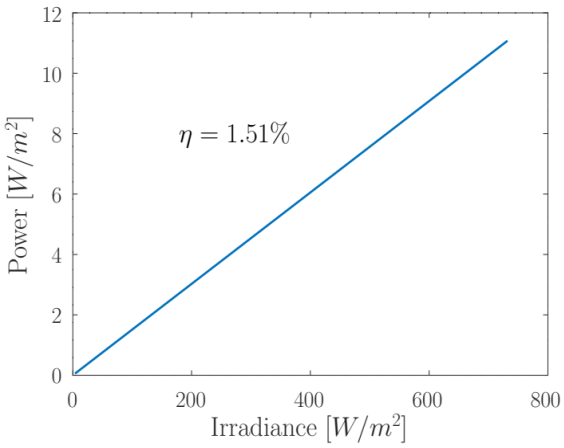

Fig.10. Device output power as a function of the irradiance

After depositing a 150nm ITO coating and adding the bus bar, fingers and back electrode, the photo-current was measured under various intensities which were controlled using a UNI-T UT383BT luxmeter. The measured illuminance was converted to irradiance based on a recent guide which tries to sort out the various conversion factors [21]. Based on their recommendation we used a 116 [$^{lux}/_{W/m^2}$]. Fig.10 displays the devices output power as a function of the irradiance.

The slope of the graph shows the efficiency of the device, which is 1.51% in the above measurement.

DISCUSSION

A recent study [22] estimates the EOL cost of a PV panel at 6.72 USD/m^2, while the cost of the actual recycling including 0.25 USD/m^2. Most of the cost consists of panel transport and processing of PV waste. We have focused on recycling single crystal wafers which are repurposed. As such, in this work we have used the standard stripping methods which are applied in microelectronics, though better, cheaper and environmentally benign methods do exist as discussed in [4]. Stripping methods are discussed extensively in literature, our work was focused on demonstrating preliminary work consisting of a simple method for doping stripped single crystalline silicon creating a PN junction. The presented efficiencies are considered low, but we have demonstrated it is a viable method, which still needs to be perfected.

CONCLUSIONS

This work presents a viable method for recycling and re-purposing used silicon wafers for PV use. The preliminary work shows that standard stripping methods followed by a newly suggested method for diffusing dopants does provide a working PV cell. Both optical and electrical properties of the resulting device were presented. The output power density's dependence on the incident irradiance resulted in a 1.51 % efficiency, which is an order of magnitude lower than expected. As this work was intended as a feasibility study, the result shows promise. Following this work we intend to improve the efficiency of a single crystal wafer cell and present a method for assembling an efficient solar panel from the salvaged wafers. In the future we will extend this work to recycling polycrystalline wafers which are abundant in the ever increasing retired solar panels.

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